REMARKS

Applicants gratefully acknowledge the Examiner's indication that claims 3, 8, 9, 14, 17 – 22, and 26 contain allowable subject matter. Applicants note that claim 27 depends upon claim 26 and is thus also allowable.

A terminal disclaimer is enclosed to overcome the nonstatutory obviousness-type double patenting rejection over US Pat. No. 6,653,861.

Applicants respectfully traverse the indefiniteness rejection of claims 10, 23, and 24. Claim 10 recites a plurality of I/O blocks. In addition, claim 10 limits each I/O block to include "at least two I/O cells, each I/O cell including a multiplexer..." Since there are at least two I/O blocks recited by such a claim, there must be at least four multiplexers (since each I/O block includes two I/O cells, each I/O cell including a multiplexer). Accordingly, there is inherent antecedent basis to later recite "the multiplexers" in claim 10. Claims 23 and 24 are also definite for the same reasons.

Applicants traverse the rejections of claim 1, 2, 4 – 7, and 10 – 26 as being anticipated by the Lacey reference (USP 6,864,710). In that regard, consider the function of a programmable interconnect circuit such as shown in Applicants' Figures 2 and 3. A user may program or configure this interconnect circuit such that any pin 20 (Figure 3) may be connected to any other pin in the device (hence the name "programmable interconnect" circuit). For example, programmable interconnect circuits may be employed in a "bus switching" application so that one bus of signals may be switched into another bus of signals depending upon the programming of the programmable interconnect circuit.

Applicants have provided a particularly advantageous architecture for applications such as bus-switching. As described by the Applicants on, for example, page 5, line 15 through page 6, line 8, a plurality of I/O circuits are arranged into I/O blocks. Each I/O block corresponds to its own routing structure that receives signals from all the pins in the device.

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Each routing structure may programmably route the received signals to the I/O circuits in the I/O block corresponding to the routing structure.

Claim 1 reflects this advantageous "block-oriented" programmable interconnect architecture in that it recites, for example, a "a plurality of N routing structures corresponding to the plurality of N I/O blocks, each routing structure configured to receive signals from the plurality of I/O cells and programmable route the signals to each I/O cell within the routing structure's I/O block."

The Lacey reference stands in sharp contrast. For example, Lacey's Figure 1 illustrates a conventional programmable logic device architecture, having vertical routing structures 106 and horizontal routing structures 104. As known in the programmable logic device arts, a horizontal routing structure such as 104a typically includes segmented wires that span various numbers of columns. Similarly, a vertical routing structure such as 106a typically includes segmented wires that span various number of rows. Fuse points at the intersections of vertical and horizontal wires allow the routing of signals from an I/O block to logic elements 102. Similar fuse points allow the routing of signals from one logic element to another as well as to particular I/O blocks. Such routing is conventional for many types of programmable logic devices. But what is not conventional and not taught or suggested by the Lacey is an architecture wherein each I/O block has its own routing structure that may receive signals from any pin on the device and programmably route the received signals to I/O cells within its I/O block. Accordingly, claim 1 and its dependent claims are allowable over Lacey.

Claim 10 has been amended to recite a plurality of routing structures. Thus claim 10 and its dependent claims are allowable over Lacey for analogous reasons. Claim 13 is cancelled. Claims 14 through 21 are amended in light of the amendment to claim 10. No new matter is added.

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Claim 23 is allowable for analogous reasons as discussed with regard to claim 1.

Claim 24 has been amended to recite a plurality of routing structures. Thus, claim 24 and its dependent claims are allowable for analogous reasons as discussed with regard to claim 1. Claim 25 is cancelled. Claims 26 and 27 are amended in light of the amendment to claim 24. No new matter is added.

CONCLUSION

For the above reasons, the pending claims are in condition for allowance and allowance of the application is hereby solicited. If the Examiner has any questions or concerns, a telephone call to the undersigned at 949 752 7040 is welcomed and encouraged.

Certificate of Transmission

I hereby certify that this correspondence is being sent via First Class Mail to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22303-1450, Mail Stop Amendment on the date stated below.

Tina Kavanaugh /tk/ February 23, 2006

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